IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A method of controlling a process performed by a semiconductor processing tool, comprising:

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

inputting process data related to an actual process being performed by the semiconductor processing tool;

setting boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool;

storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

solving the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by:

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;

providing from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result; and

using the first principles simulation result obtained during performance of the actual process to build an empirical model; and

selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool.

Claim 2 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises directly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

Claim 3 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises indirectly inputting the data relating to the actual process being performed by the semiconductor processing tool from at least one of a manual input device and a database.

Claim 4 (Original): The method of Claim 3, wherein said indirectly inputting comprises inputting data recorded from a process previously performed by the semiconductor processing tool.

Claim 5 (Original): The method of Claim 3, wherein said indirectly inputting comprises inputting data set by a simulation operator.

Claim 6 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

Claim 7 (Previously Presented): The method of Claim 1, wherein said inputting process data comprises inputting data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

Claim 8 (Canceled).

Claim 9 (Previously Presented): The method of Claim 1, wherein said inputting a first principles physical model comprises inputting fundamental equations as the set of computer-encoded differential equations necessary to perform first principles simulation for a desired simulation result.

Claim 10 (Canceled).

Claim 11 (Previously Presented): The method of Claim 1, further comprising performing first principles simulation independent of the process performed by the semiconductor processing tool.

Claims 12-13 (Canceled).

Claim 14 (Original): The method of Claim 1, wherein said using the first principles simulation result comprises using the first principles simulation result to control the process performed by the semiconductor processing tool.

Claim 15 (Original): The method of Claim 1, further comprising using a network of interconnected resources to perform at least one of the process steps recited in Claim 1.

Claim 16 (Original): The method of Claim 15, further comprising using code parallelization among interconnected computational resources to share the computational load of the first principles simulation.

Claim 17 (Original): The method of Claim 15, further comprising sharing simulation information among interconnected resources to control the process performed by the semiconductor processing tool.

Claim 18 (Original): The method of Claim 17, wherein said sharing simulation information comprises distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources.

Claim 19 (Original): The method of Claim 17, wherein said sharing simulation information comprises distributing model changes among the interconnected resources to reduce redundant refinements of first principles simulations by different resources.

Claim 20 (Original): The method of Claim 15, further comprising using remote resources via a wide area network to control the semiconductor process performed by the semiconductor processing tool.

Claim 21 (Previously Presented): The method of Claim 20, wherein said using remote resources comprises using at least one of remote computational and storage resources via a wide area network to control the semiconductor process performed by the semiconductor processing tool.

Claim 22 (Original): The method of Claim 1, wherein said performing first principles simulation utilizes at least one of an ANSYS computer code, a FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

Claim 23 (Original): The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 24 (Original): The method of Claim 23, wherein said using the first principles simulation result to control comprises:

controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

Claim 25 (Original): The method of Claim 1 wherein said inputting data comprises:

inputting at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension, an etch feature anisotropy, a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

Claim 26 (Original): The method of Claim 1, wherein said inputting data comprises:

inputting physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system , a deposition system , a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 27 (Original): The method of Claim 1, wherein said using the first principles simulation result to control comprises:

controlling the semiconductor processing tool by using empirical model output to adjust said process performed by the semiconductor processing tool.

Claim 28 (Currently Amended): A system comprising:

a semiconductor processing tool configured to perform a process;

a fab-level library storing known simulation results obtained from simulation modules in a device manufacturing fab;

a fab-level process controller distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

a first principles simulation processor configured to input a first principles physical model including a set of computer-encoded differential equations describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

an input device configured to input process data related to an actual process being performed by the semiconductor processing tool; and

said first principles simulation processor further configured to:

set boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool,

solve the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by:

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module, and

provide from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result, and

use the first principles simulation result obtained during performance of the actual process to build an empirical model, wherein at least one of said first principles simulation result and said empirical model is selected to control the actual process being performed by the semiconductor processing tool.

Claim 29 (Original): The system of Claim 28, wherein said input device comprises at least one of a physical sensor and a metrology tool physically mounted on the semiconductor processing tool.

Claim 30 (Original): The system of Claim 28, wherein said input device comprises at least one of a manual input device and a database.

Claim 31 (Original): The system of Claim 30, wherein said input device is configured to input data recorded from a process previously performed by the semiconductor processing tool.

Claim 32 (Original): The system of Claim 30, wherein said input device is configured to input data set by a simulation operator.

Claim 33 (Original): The system of Claim 28, wherein said input device is configured to input data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment.

Claim 34 (Original): The system of Claim 28, wherein said input device is configured to input data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool.

Claim 35 (Canceled).

Claim 36 (Previously Presented): The system of Claim 28, wherein said processor is configured to input a first principles physical model comprising fundamental equations as the set of computer-encoded differential equations necessary to perform first principles simulation for a desired simulation result.

Claims 37-40 (Canceled).

Claim 41 (Original): The system of Claim 28, wherein said processor is configured to use the first principles simulation result to control the process performed by the semiconductor processing tool.

Claim 42 (Original): The system of Claim 28, further comprising a network of interconnected resources connected to said processor and configured to assist said processor in performing at least one of the inputting a first principles simulation model and performing a first principles simulation.

Claim 43 (Original): The system of Claim 42, wherein said network of interconnected resources is configured to use code parallelization with said processor to share the computational load of the first principles simulation.

Claim 44 (Original): The system of Claim 42, wherein said network of interconnected resources is configured to share simulation information with said processor to facilitate said process performed by the semiconductor processing tool.

Claim 45 (Original): The system of Claim 44, wherein said network of interconnected resources is configured to distribute simulation results to said processor to reduce redundant execution of substantially similar first principles simulations.

Claim 46 (Original): The system of Claim 44, wherein said network of interconnected resources is configured to distribute model changes to said processor to reduce redundant refinements of first principles simulations.

Claim 47 (Original): The system of Claim 42, further comprising remote resources connected to said processor via a wide area network and configured to facilitate the semiconductor process performed by the semiconductor processing tool.

Claim 48 (Original): The system of Claim 47, wherein said remote resources comprise at least one of a computational and a storage resource.

Claim 49 (Original): The system of Claim 28, wherein said processor is configured to perform first principles simulation by utilizing at least one of an ANSYS computer code, a FLUENT computer code, a CFRDC-ACE computer code, and a direct simulation Monte Carlo computer code.

Claim 50 (Original): The system of Claim 28, wherein said processor is configured to use the first principles simulation result to control by controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 51 (Original): The system of Claim 50, wherein said processor is configured to use the first principles simulation result to control by controlling at least one of a chemical vapor deposition system and a physical vapor deposition system.

Claim 52 (Original): The system of Claim 28, wherein said processor is configured to input at least one of etch rate, deposition rate, etch selectivity, an etch critical dimension, an etch feature anisotropy, a film property, a plasma density, an ion energy, a concentration of a chemical specie, a photoresist mask film thickness, a photoresist pattern dimension.

Claim 53 (Original): The system of Claim 28, wherein said processor is configured to input physical geometric parameters of at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace.

Claim 54 (Original): The system of Claim 28, wherein said processor is configured to use the first principles simulation result to control by controlling the semiconductor processing tool by using empirical model output to adjust said process performed by the semiconductor processing tool.

Claims 55-57 (Cancelled)

Claim 58 (Currently Amended): At least one of non-volatile media and volatile media containing program instructions for execution on a processor, which when executed by the computer system, cause the processor to perform the steps of:

inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

inputting process data related to an actual process being performed by the semiconductor processing tool;

setting boundary conditions for the spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool;

storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

solving the computer-encoded differential equations of the first principles physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed to produce a first principles simulation by:

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;

providing from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result; and

using the first principles simulation result obtained during performance of the actual process to build an empirical model; and

selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool.

Claims 59 -61 (Cancelled).